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IN THE CLAIMS

Amend the claims as follows. All pending claims are shown in accordance with Rule 1.121 § (1)(i).

Withdraw claims 23-32 without prejudice to the subject matter thereof.

33. (Currently amended) An amplifier, comprising:

a gain stage having [first and second]an input[s] for receiving an[differential] input signal and first and second outputs for providing a differential amplified signal; and

an output stage including first and second depletion mode transistors operating in response to the differential amplified signal and serially coupled between a supply terminal and an output of the amplifier for providing an output signal.

34. (Currently amended) The amplifier of claim 33, further comprising a feedback path from the output of the amplifier to the [first]input of the gain stage to reduce the gain of the amplifier.

35. (Currently amended) The amplifier of claim 34, wherein the feedback path includes:

a first resistor coupled between the output of the amplifier and the [first]input of the gain stage; and

a second resistor coupled from the [first]input of the gain stage to a reference node.

36. (Currently amended) The amplifier of claim 35 for functioning as a voltage regulator, wherein the[differential] input signal includes a reference voltage applied to the second

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input of the gain stage to maintain the output signal at a constant potential.

37. (Previously added) The amplifier of claim 36, wherein a difference between a supply voltage at the supply terminal and the constant potential of the output signal is less than 0.2 volts.

38. (Previously added) The amplifier of claim 33, wherein the first depletion mode transistor is an n-channel device having a drain coupled to the supply terminal and a source coupled to a node, and the second depletion mode transistor is a p-channel device having a source coupled to the node and a drain coupled to the output of the amplifier.

39. (Previously added) The amplifier of claim 33, further comprising a level shift circuit having first and second inputs for level shifting the differential amplified signal by a predefined potential to provide a differential level shifted signal at first and second outputs of the level shift circuit.

40. (New) The amplifier of claim 39, wherein the first depletion mode transistor has a gate coupled to the first output of the level shift circuit and the second depletion mode transistor has a gate coupled to the second output of the level shift circuit.